BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of: Mark S. Chang et al.

Serial No.: 09/539,458

Filed: March 30, 2000

Group Art Unit: 2814

Before the Examiner: Pham, H.

Title: METHOD AND SYSTEM FOR PROVIDING CONTACT TO A FIRST POLYSILICON LAYER IN A FLASH MEMORY DEVICE

APPEAL BRIEF

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

I. REAL PARTY IN INTEREST

The real party in interest is Advanced Micro Devices, Inc., which is the assignee of the entire right, title and interest in the above-identified patent application.

CERTIFICATION UNDER 37 C.F.R. §1.8

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to Mail Stop Appeal Brief-Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on April 6, 2005.

Serena Beller
Signature

Serena Beller
(Printed name of person certifying)

II. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences known to Appellants, Appellants' legal representative or assignee which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 1-3 and 17-21 are pending in the Application. Claim 21 is allowed. Claims 1-3 and 17-20 stand rejected. Claims 1-3 and 17-20 are appealed.

IV. STATUS OF AMENDMENTS

The Appellants' response to the Office Action having a mailing date of December 21, 2004, has been considered, but the Examiner indicated that it did not place the application in condition for allowance because Appellants' arguments were deemed unpersuasive.

V. SUMMARY OF CLAIMED SUBJECT MATTER

In one embodiment of the present invention, a flash memory device may comprise a plurality of gate stacks including a plurality of floating gates and a plurality of control gates disposed on a semiconductor substrate. Specification, page 8, lines 15-19; Specification, page 14, claim 1, lines 1-3; Figure 3B, elements 200, 210, 212 and 216. The flash memory device may further comprise at least one component including a polysilicon layer having a top surface, where the at least one component is formed on a field oxide region configured to separate the plurality of gate stacks. Specification, page 9, lines 1-2; Specification, page 14, claim 1, line 4; Figure 3B, element 226. The flash memory device may further comprise a silicide on the top surface of the polysilicon layer of the at least one component. Specification, page 9, lines 4-5; Specification, page 14, claim 1, line 5; Figure 3B,

element 228. The flash memory device may further comprise an insulating layer covering the plurality of gate stacks, the at least one component and the silicide, the insulating layer having a plurality of contact holes therein. Specification, page 9, lines 5-8; Specification, page 14, claim 1, lines 6-7; Figure 3B, elements 210, 226, 228, 230, 232, 234 and 236.

In another embodiment of the present invention, a flash memory device comprises an oxide layer. Specification, page 8, line 17; Figure 3B, element 205. The flash memory device may further comprise a gate stack formed on the oxide layer where the gate stack comprises a first polysilicon layer, an insulating layer formed on the first polysilicon layer and a second polysilicon layer formed on the insulating layer. Specification, page 8, lines 16-23; Figure 3B, elements 210, 212, 214, 216. The flash memory device may further comprise a field oxide region located adjacent to the oxide layer. Specification, page 8, lines 16-18; Figure 3B, elements 204, 205. The flash memory device may further comprise a component located on said field oxide region where the component is formed from one of the first and second polysilicon layers. Specification, page 9, lines 1-4; Figure 3B, elements 204, 212, 216, 226. The flash memory device may further comprise a silicide layer formed on said component. Specification, page 9, lines 4-5; Figure 3B, elements 226, 228.

In another embodiment of the present invention, a flash memory device comprises an oxide layer. Specification, page 8, line 17; Figure 3B, element 205. The flash memory device may further comprise a gate stack formed on the oxide layer where the gate stack comprises a first polysilicon layer, an insulating layer formed on the first polysilicon layer and a second polysilicon layer formed on the insulating layer. Specification, page 8, lines 16-23; Figure 3B, elements 210, 212, 214, 216. The flash memory device may further comprise a field oxide region located adjacent to the oxide layer. Specification, page 8, lines 16-18; Figure 3B, elements 204, 205. The flash memory device may further comprise a component located on

said field oxide region where the component is formed from one of the first and second polysilicon layers. Specification, page 9, lines 1-4; Figure 3B, elements 204, 212, 216, 226. The flash memory device may further comprise a silicide layer formed on said component where the component comprises a resistor. Specification, page 9, lines 4-5; Specification, page 1, lines 17-18; Figure 3B, elements 226, 228.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1, 17 and 18 stand rejected under 35 U.S.C. §102(e) as being anticipated by Lee et al. (U.S. Patent No. 6,197,639) (hereinafter "Lee"). Claims 2, 3, 19 and 20 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Lee in view of Ma et al. (U.S. Patent No. 5,939,753) (hereinafter "Ma").

VII. ARGUMENT

A. Claims 1, 17 and 18 are not properly rejected under 35 U.S.C. §102(e) as being anticipated by Lee.

The Examiner has rejected claims 1, 17 and 18 under 35 U.S.C. §102(e) as being anticipated by Lee. Paper No. 19, page 2. Appellants respectfully traverse these rejections for at least the reasons stated below.

For a claim to be anticipated under 35 U.S.C. §102, each and every claim limitation must be found within the cited prior art reference and arranged as required by the claim. M.P.E.P. § 2131.

1. Claim 1 is not anticipated by Lee.

Appellants respectfully assert that Lee does not disclose "at least one component including a polysilicon layer having a top surface, wherein the at least one component is formed on a field oxide region configured to separate the plurality of

gate stacks" as recited in claim 1. The Examiner cites elements 57, 63 of Lee as disclosing an at least one component. Paper No. 19, page 2. The Examiner further cites element 53 of Lee as disclosing a field oxide region. Paper No. 19, page 2. Appellants respectfully traverse the assertion that Lee discloses the above-cited claim limitation.

Lee instead discloses that a field oxide layer 53 is formed on a silicon substrate 51 to define an active region. Column 3, lines 40-41. Lee further discloses that a tunnel oxide layer 55 is formed on the silicon substrate 51 having the field oxide layer 53 and the active region, to a thickness of 100Å. Column 3, lines 41-44. Lee further discloses that a first polysilicon layer 57 for forming a floating gate is formed on the tunnel oxide layer 55. Column 3, lines 44-45. Lee further discloses that after forming a gate oxide layer 61 in the periphery region, a second polysilicon layer 63 and a tungsten silicide layer 65, as a control gate, are formed in the cell array region and the periphery region. Column 3, line 65 – column 4, line 1. As illustrated in Figure 6, second polysilicon layer 63 is formed on ONO layer 58. There is no language in Lee that discloses that polysilicon layers 57, 63 are a component. Neither is there any language in Lee that discloses that polysilicon layers 57, 63 are formed on a field oxide region. Thus, Lee does not disclose all of the limitations of claim 1, and thus Lee does not anticipate claim 1. M.P.E.P. §2131.

Appellants further assert that Lee does not disclose "a silicide on the top surface of the polysilicon layer of the at least one component", as recited in claim 1, for at least the reasons stated above.

Appellants further assert that Lee does not disclose "an insulating layer covering the plurality of gate stacks, the at least one component and the silicide, the insulating layer having a plurality of contact holes therein", as recited in claim 1, for at least the reasons stated above.

2. Claims 17 and 18 are not anticipated by Lee.

As stated above, for a claim to be anticipated under 35 U.S.C. §102, each and every claim limitation must be found within the cited prior art reference and arranged as required by the claim. M.P.E.P. § 2131.

Appellants respectfully assert that Lee does not disclose "a component located on said field oxide region, wherein said component is formed from one of said first and said second polysilicon layer" as recited in claim 17. The Examiner cites elements 57, 63 of Lee as disclosing a component. Paper No. 19, page 3. Appellants respectfully traverse the assertion that Lee discloses the above-cited claim limitation.

Lee instead discloses that a gate stack that includes both the first and second polysilicon layers (elements 57 and 63) is formed on field oxide layer 53 as illustrated in Figure 7. Claim 17 recites both a gate stack and a component. Under the rule of claim differentiation, a gate stack may not be interpreted as a component. Furthermore, the gate stack is not formed from one of the first and second polysilicon layers, as required by claim 17, but from both of the first and second polysilicon layers. Thus, Lee does not disclose a component located on the field oxide region, where the component is formed from one of the first and second polysilicon layers. Hence, Lee does not disclose all of the limitations of claim 17, and thus Lee does not anticipate claim 17. M.P.E.P. §2131.

Appellants further assert that Lee does not disclose "a silicide layer formed on said component", as recited in claim 18, for at least the reasons stated above.

Claim 18 recites combinations of features including the combinations of claim 17, and thus is not anticipated for at least the reasons claim 17 is allowable.

B. Claims 2, 3, 19 and 20 are not properly rejected under 35 U.S.C. §103(a) as being unpatentable over Lee in view of Ma.

The Examiner has rejected claims 2, 3, 19 and 20 under 35 U.S.C. §103(a) as being unpatentable over Lee in view of Ma. Paper No. 19, page 4. Appellants respectfully traverse these rejections for at least the reasons stated below and respectfully request that the Examiner reconsider and withdraw these rejections.

1. The Examiner has not presented a source of motivation for modifying Lee with Ma.

The Examiner admits that Lee does not teach a silicide layer formed on a component that includes either titanium silicide or cobalt silicide, as recited in claims 2-3 and 19-20. Paper No. 19, page 4. The Examiner states that the motivation to modify Lee with Ma to have a silicide layer formed on a component that includes either titanium silicide or cobalt silicide, as recited in claims 2-3 and 19-20, is because "such materials are equivalence for their use in the semiconductor art as to form a dual-layer structure with low resistance, which is made up of a polysilicon and metal silicide." Paper No. 19, page 5. The motivation to modify Lee with Ma must come from one of three possible sources: the nature of the problem to be solved, the teachings of the prior art, and the knowledge of persons of ordinary skill in the art. *In re Rouffet*, 149 F.3d 1350, 1357, 47 U.S.P.Q.2d 1453, 1457-58 (Fed. Cir. 1998). The Examiner has not provided any evidence that his motivation comes from any of these sources. Instead, the Examiner is relying upon his own subjective opinion which is insufficient to support a *prima facie* case of obviousness. *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002). Consequently, the Examiner's motivation is insufficient to support a *prima facie* case of obviousness for rejecting claims 2, 3, 19 and 20. *Id.*

2. By modifying Lee with Ma, the principle of operation of Lee would change.

If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious. *In re Ratti*, 370 F.2d 810, 123 U.S.P.Q. 349 (C.C.P.A. 1959). Further, if the proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. *In re Gordon*, 733 F.2d 900, 221 U.S.P.Q. 1125 (Fed. Cir. 1984). For the reasons discussed below, Appellants submit that by modifying Lee with Ma, the principle of operation in Lee would change and subsequently render the operation of Lee to perform its purpose unsatisfactorily.

Lee teaches a floating gate formed of the first polysilicon layer pattern 57a, a dielectric layer pattern 58a, a control gate including a silicide layer pattern 65a and a second polysilicide layer 63a, an anti-reflective layer pattern 67a and a nitride layer pattern 69a are formed, thereby completing a stack gate in the cell array region of the silicon substrate 51. Column 4, lines 18-24. As illustrated in Figure 6, the silicide layer pattern 65a covers the entire second polysilicide layer 63a. Lee further teaches that over-etching occurs because the step difference in the cell array region is larger than the step difference in the periphery region. Column 1, lines 61-63. Lee further teaches fabricating a NOR flash memory device, capable of reducing etching damage, which also simplifies a process for forming a contact region of a cell array region and a periphery region. Column 1, line 67 – column 2, line 3.

Ma, on the other hand, teaches titanium silicide regions that cover portions of polysilicon resistor 58 as illustrated in Figure 7. Column 7, lines 48-51.

By combining Lee with Ma, Lee would no longer be able to reduce etching damage as the silicide layer pattern 65a would no longer cover the entire second polysilicide layer 63a. As stated above, Ma teaches that the silicide covers portions of

a polysilicon resistor. Hence, by combining Lee with Ma, the silicide layer 65a in Lee would no longer cover the entire polysilicide layer 63a but only portions of the second polysilicide layer 63a. By modifying Lee so that the silicide layer 65a covers portions of the second polysilicide layer 63a, Lee would not be able to reduce etching damage, which is the principle of operation of Lee. Thus, by modifying Lee with Ma, the principle of operation in Lee would change, and subsequently render the operation of Lee to perform its purpose unsatisfactorily. Therefore, the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 2, 3, 19 and 20. *In re Ratti*, 270 F.2d 810, 123 U.S.P.Q. 349 (C.C.P.A. 1959); *In re Gordon*, 733 F.2d 900, 221 U.S.P.Q. 1125 (Fed. Cir. 1984).

The Examiner, in response to Appellants' assertion that the principle of operation of Lee would change by combining Lee with Ma, asserts that the reference Ma does not need to be considered in its entirety in an obviousness rejection. Paper No. 19, page 7. Appellants respectfully traverse. The entire Ma reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention as discussed above. *W.L. Gore & Associates, Inc. v. Garlock, Inc.*, 220 U.S.P.Q. 303 (Fed. Cir. 1983); M.P.E.P. §2141.02. Accordingly, the Examiner must consider the <u>entire</u> Ma reference and not just the aspect of Ma teaching silicide material.

3. <u>The Examiner has not presented any objective evidence for modifying Lee with Ma.</u>

A *prima facie* showing of obviousness requires the Examiner to establish, *inter alia*, that the prior art references teach or suggest, either alone or in combination, all of the limitations of the claimed invention, and the Examiner must provide a motivation or suggestion to combine or modify the prior art reference to make the claimed inventions. M.P.E.P. §2142. The showings must be clear and

particular and supported by objective evidence. *In re Lee*, 277 F.3d 1338, 1343, 61 U.S.P.Q.2d 1430, 1433-34 (Fed. Cir. 2002); *In re Kotzab*, 217 F.3d 1365, 1370, 55 U.S.P.Q.2d 1313, 1317 (Fed. Cir. 2000); *In re Dembiczak*, 50 U.S.P.Q.2d. 1614, 1617 (Fed. Cir. 1999). Broad conclusory statements regarding the teaching of multiple references, standing alone, are not evidence. *Id*

As stated above, the Examiner's motivation for modifying Lee with Ma to have a silicide layer formed on a component include either titanium silicide or cobalt silicide, as recited in claims 2-3 and 19-20, is because "such materials are equivalence for their use in the semiconductor art as to form a dual-layer structure with low resistance, which is made up of a polysilicon and metal silicide." Paper No. 19, page 5. The Examiner's motivation is insufficient to support a *prima facie* case of obviousness for at least the reasons stated below.

The Examiner's motivation does not address as to why one of ordinary skill in the art with the primary reference (Lee) in front of him would have been motivated to modify Lee with the teachings of the secondary reference (Ma). Lee teaches a control gate that includes a silicide layer pattern 65a that covers the entire second polysilicide layer 63a. Column 4, lines 20-21 and Figure 6. As stated above, Ma teaches titanium silicide regions that cover portions of polysilicon resistor 58 as illustrated in Figure 7. Column 7, lines 48-51. Stating that titanium silicide or cobalt silicide are equivalent materials does not address as to why one of ordinary skill in the art would modify Lee with Ma such that the silicide layer (silicide layer pattern 65a), as taught in Lee, which may include titanium or cobalt silicide, would cover a portion and not the entire polysilicide layer 63a since Ma teaches silicide regions that cover portions of polysilicon resistor 58. The Examiner must provide a suggestion or motivation, either in the references or in the knowledge generally available to one of ordinary skill in the art to modify the silicide layer (silicide layer pattern 65a), as taught in Lee, which may include titanium or cobalt silicide, to cover only a portion and not the entire

polysilicide layer 63a. M.P.E.P. §2143. As the Examiner has not provided such motivation, but instead relies upon his own subjective opinion, the Examiner has not presented a *prima facie* case of obviousness in rejecting claims 2, 3, 19 and 20. *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002); M.P.E.P. §2143.

4. The Examiner has not presented a reasonable expectation of success when combining Lee with Ma.

The Examiner must present a reasonable expectation of success in combining Lee with Ma in order to establish a *prima facie* case of obviousness. M.P.E.P. §2143.02.

Lee teaches fabricating a NOR flash memory device, capable of reducing etching damage, which also simplifies a process for forming a contact region of a cell array region and a periphery region. Column 1, line 67 – column 2, line 3. Ma, on the other hand, teaches a monolithic integrated circuit and a process for fabricating the monolithic integrated circuit that performs both radio frequency analog circuit and digital circuit functions. Column 1, line 65 – column 2, line 27. The Examiner has not presented any evidence that there would be a reasonable expectation of success in combining Lee, that relates to a NOR flash memory device with reduced etching damage, with Ma, that relates to a monolithic integrated circuit that performs both radio frequency analog circuit and digital circuit functions. The Examiner must provide objective evidence as to how a NOR flash memory device with reduced etching damage would be combined with a monolithic integrated circuit that performs both radio frequency analog circuit and digital circuit functions. M.P.E.P. §2143.02. Since the Examiner has not provided such evidence, the Examiner has not presented a reasonable expectation of success in combining Lee with Ma. M.P.E.P. §2143.02. Accordingly, the Examiner has not presented a *prima facie* case of obviousness in rejecting claims 2, 3, 19 and 20. M.P.E.P. §2143.02.

VIII. CONCLUSION

For the reasons noted above, the rejections of claims 1-3 and 17-20 are in error. Appellants respectfully request reversal of the rejections and allowance of claims 1-3 and 17-21.

Respectfully submitted,
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APPENDIX

1. A flash memory device comprising:

a plurality of gate stacks including a plurality of floating gates and a plurality of control gates disposed on a semiconductor substrate;

at least one component including a polysilicon layer having a top surface, wherein the at least one component is formed on a field oxide region configured to separate the plurality of gate stacks;

a silicide on the top surface of the polysilicon layer of the at least one component; and

an insulating layer covering the plurality of gate stacks, the at least one component and the silicide, the insulating layer having a plurality of contact holes therein.

2. The flash memory device of claim 1 wherein the silicide further includes a titanium silicide.

3. The flash memory device of claim 1 wherein the silicide further includes a cobalt silicide.

17. A flash memory device, comprising:

an oxide layer;

a gate stack formed on said oxide layer, wherein said gate stack comprises:

a first polysilicon layer;

an insulating layer formed on said first polysilicon layer; and

a second polysilicon layer formed on said insulating layer;

a field oxide region located adjacent to said oxide layer;

a component located on said field oxide region, wherein said component is formed from one of said first and said second polysilicon layer; and

a silicide layer formed on said component.

18. The flash memory device as recited in claim 17, wherein said silicide layer on said component prevents etching through one of said first and said second polysilicon layer.

19. The flash memory device as recited in claim 17, wherein said silicide layer comprises a titanium silicide.

20. The flash memory device as recited in claim 17, wherein said silicide layer comprises a cobalt silicide.

21. A flash memory device, comprising:

an oxide layer;

a gate stack formed on said oxide layer, wherein said gate stack comprises:

a first polysilicon layer;

an insulating layer formed on said first polysilicon layer; and

a second polysilicon layer formed on said insulating layer;

a field oxide region located adjacent to said oxide layer;

a component located on said field oxide region, wherein said component is formed from one of said first and said second polysilicon layer; and

a silicide layer formed on said component;

wherein said component comprises a resistor.

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TRANSMITTAL FORM

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Total Number of Pages in This Submission: 16

Application Number	09/539,458
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First Named Inventor	Mark S. Chang et al.
Art Unit	2814
Examiner Name	H. Pham
Attorney Docket Number	DA01028

ENCLOSURES *(Check all that apply)*

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Firm Name	Winstead Sechrest & Minick P.C.		
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Date	April 6, 2005	Reg. No.	47,159

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FEE TRANSMITTAL
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☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) **500.00**

Complete if Known	
Application Number	09/539,458
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First Named Inventor	Mark S. Chang et al.
Examiner Name	H. Pham
Art Unit	2814
Attorney Docket No.	DA01028

METHOD OF PAYMENT (check all that apply)

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Deposit Account Number: 01-0365

Deposit Account Name: Advanced Micro Devices, Inc.

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Fee Description	Fee ($)	Small Entity Fee ($)	Fee Paid($)
Utility Filing Fee	790	395	
Design Filing Fee	350	175	
Plant Filing Fee	550	275	
Reissue Filing Fee	790	395	
Provisional Filing Fee	160	80	

Subtotal (1) $ _____

FEE CALCULATION (continued)

2. EXTRA CLAIM FEES

Fee Description	Fee ($)	Small Entity Fee ($)
Each claim over 20	50	25
Each independent claim over 3	200	100
Multiple dependent claims	360	180
For Reissues, each claim over 20 and more than in the original patent	50	25
For Reissues, each independent claim more than in the original patent	200	100

Total Claims	Extra Claims	Fee ($)	Fee Paid ($)
_____ - 20 or HP =	_____	x _____	= _____

HP = highest number of total claims paid for, if greater than 20

Indep. Claims	Extra Claims	Fee ($)	Fee Paid ($)
_____ - 3 or HP =	_____	x _____	= _____

HP = highest number of independent claims paid for, if greater than 3

Multiple Dependent Claims	Fee ($)	Fee Paid ($)
	_____	_____

Subtotal (2) $ _____

3. OTHER FEES

Fee Description	Fee ($)	Small Entity Fee ($)	Fee Paid($)
1-month extension of time	120	60	
2-month extension of time	450	225	
3-month extension of time	1,020	510	
4-month extension of time	1,590	795	
5-month extension of time	2,160	1,080	
Information disclosure stmt. fee	180	180	
37 CFR 1.17(q) processing fee	50	50	
Non-English specification	130	130	
Notice of Appeal	500	250	
Filing a brief in support of appeal	500	250	500.00
Request for oral hearing	1,000	500	
Other: _____			

Subtotal (3) $ 500.00

SUBMITTED BY

Signature		Registration No. (Attorney/Agent) 47.159	Telephone 512.370.2832
Name (Print/Type)	Robert A. Voigt, Jr.		Date April 6, 2005